Towards Single Tapeout Crystal Free IoT Mote Design: Investigating Free Running Oscillator Simulation Inaccuracies

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***Abstract*—Crystal-free communication is the next step towards low-power sustainable Internet of Things (IoT) devices. Local Oscillator (LO) stability is paramount for optimal performance in RF communication systems. Frequency fluctuations in the LO can not only result in reciprocal mixing in narrowband communication systems, but it can also cause carrier mismatches between the transmitter and receiver, resulting in higher guard times and Bit Error Rates (BER); even in the absence of adjacent channels. While traditional communication systems rely on high-quality crystal oscillators and Phase-Locked Loops (PLLs) to maintain frequency stability, the power and area constraints, and battery-less nature of IoT motes necessitate the elimination of the crystal reference and PLL. Consequently, there is a growing demand for low-power free-running oscillators that are stable enough to meet the requirements of modern communication standards such as IEEE 802.15.4 and Bluetooth Low-Energy (BLE). However, the design of free-running oscillators is especially challenging due to the long simulation times, and the number of tapeout iterations required to meet the specifications. Not only does the oscillator have a non-linear large signal behavior, but the effects of flicker noise at frequencies close to the carrier are often masked in the simulations due to the Lorentzian tappering; primarily because this region is expected to be dealt with by the PLL. By investigating the simulation inaccuracies involved in the early stages of free-running oscillator design, we aim to assist designers in getting their first tapeout to meet the desired specifications, thereby reducing the number of tapeouts required as well as the environmental impact that they may have.**

***Index Terms*—IoT motes, RF Oscillator, phase noise**

I. Introduction

The goal of crystal-free IoT devices is to eliminate the need for the crystal reference and Phased Lock Loop (PLL) to reduce the power consumption and area utilization of IoT devices. By eliminating the crystal reference and only using free-running on-chip oscillators for both time keeping and RF communication, the power consumption of the IoT mote may be reduced significantly. To that end, low-power on-chip oscillators that can satisfy the frequency stability/phase noise criteria of communication standards such as IEEE 802.15.4 O-QPSK/MSK PHY [1] and Bluetooth Low-Energy (BLE) [2] are needed. However, the design of high quality on-chip oscillators is a challenging task owing to the long transient simulation times required and the number of simulation pitfalls that may surprise the designer. This is primarily due to the oscillator's large signal behavior, and its non-linear or Linear Time Varying (LTV) nature, which makes it difficult to use normal simulation and analysis methods. Furthermore, phase noise modeling and simulation become especially challenging at frequencies that are close to the carrier, where flicker noise starts dominating. Traditional communication systems rely on the crystal reference and PLL to mitigate the noise in these low offset regimes. However, since the goal of crystal free IoT is to eliminate the crystal reference and use a free-running oscillator, this region of noise poses significant challenges for IoT mote designers. As such, the absence of robust and reliable simulation methods, and knowledge thereof, may force the designers to run multiple tapeouts which is costly, time consuming, and environmentally hazardous.

Cadence Virtuoso is one of the most prominent analog Integrated Circuit (IC) design tools used both in industry and academia. It provides the user with a robust design environment that also includes a variety of noise simulation options, some of them specifically designed for oscillator simulations. Periodic Steady State (PSS) combined with Periodic Noise (PNoise) analysis, Harmonic Balance (HB) combined with Harmonic Balance Noise (HBNoise) analysis, and transient noise simulations are the three most attractive approaches at an oscillator designer's disposal. Among these methods, PSS/PNoise and HB/HBNoise methods are fast AC simulation methods, whereas transient noise is the slower transient simulation method that may even take several weeks to run. We found that these simulation methods may compute different phase noise profiles for the same oscillator design, which can make it difficult for the designer to have faith in them. Furthermore, in the case of the faster AC simulation methods, as the frequency offset approaches zero, the Lorentzian bound kicks in, flattening the entire phase noise profile. Upon a closer inspection, we found that other designers, have also faced similar issues, and some of them, for instance, Shawn Logan, have started coming up with ways to mitigate these simulation discrepancies [3].

The goal of this study is to investigate these simulation approaches and identify methods that can be adopted to produce fast robust simulations that can be used to model the real behavior that an oscillator in silicon may exhibit,

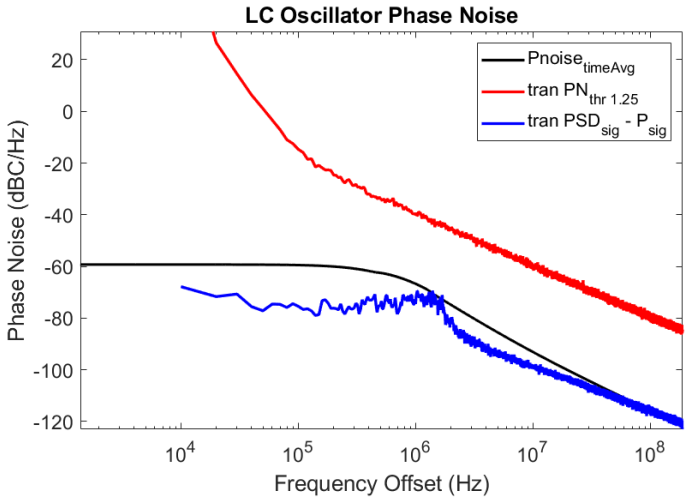

Fig. 1: Phase noise simulation results using PNoise and transient simulation methods. Using different threshold voltage results in large offsets in phase noise, and even using correct thresholds, the results show differences in the flicker noise region.

especially so at close to carrier frequencies. By resolving these discrepancies and determining the correct simulation methods, we aim to assist oscillator designers in successfully simulating their designs and meeting the desired specifications in their first tapeout. This would significantly reduce the design time as well as the environmental impact that initial design cycles of IoT motes may have.

II. Simulation Methods and Results

During our investigations, we found a few different methods to simulate oscillator phase noise. These methods and the key takeaways are discussed here.

A. PSS/Pnoise and HB/HBNoise Analysis

The PSS/Pnoise analysis method while using the time average option is outlined in the Rapid Adoption Kit (RAK) [4]. The PSS analysis determines the oscillator's steady-state response after running it for several cycles, and PNoise analysis then injects noise into the circuit and determines the resulting phase noise. Similarly, the HB analysis method determines the frequency harmonics and HBNoise proceeds to inject noise at the sidebands of all these harmonics and determines the resulting phase noise.

B. Transient Noise Analysis

The other method that is generally accepted to be much more accurate is running long transient simulations with noise and then calculating the phase noise from those results. However, these transient simulations for fast RF oscillators may take several days or even weeks. This is primarily because of the extremely small time steps and long total simulation time required for such simulations. For instance, in our experiments, running a 9 GHz oscillator, the desired $noisef_{max}$ was close to $30\,GHz$, and for measuring Allan variance up to an averaging window of $1\ ms$, the simulation time needed to be at least $10\,ms$. This results in a wide dynamic range with very small time steps and relatively large simulation time, forcing the simulator to run for several days. Thus accurate as it may be, the transient simulation approach is extremely time consuming and cannot be practically used for design purposes.

C. Results

The simulation results are summarized in Fig. 1. As can be seen from the PNoise results, indicated in black in Fig. 1, the phase noise at lower offsets, in this case close to $1MHz$, gets tapered due to the Lorentzian profile. However, for free running oscillators, this is the region of interest that cannot be ignored. The blue trace in Fig. 1 shows the results obtained by running a long transient simulation, computing the Power Spectral Density (PSD) of the signal, and subtracting the power of the fundamental frequency. The results match well with the Pnoise results for large frequency offsets, i.e., between offsets of $\approx 22\,MHz - 119\,MHz$, but as the offset gets lower, the results start differing from each other. Furthermore, the red trace in Fig. 1 shows another demonstration of calculating the phase noise from transient simulations, wherein the threshold voltage was deliberately chosen away from the actual signal DC value. As a result, the phase noise computed shows a huge offset as compared to the other results. These are all different simulation challenges that can affect the simulation accuracy, thereby forcing designers to run multiple tapeouts before meeting the specifications for their free running oscillator.

III. Conclusion

Phase noise simulation of oscillators is time consuming and different methods may produce different results at low frequency offset, i.e., close to the carrier. In order to successfully design and simulate free running oscillators, that are essential for low power crystal free IoT motes, fast and reliable simulation methods that can be trusted are needed. In this study, we examine the different simulation methods that a designer can use to ensure robust simulation of free running oscillators.

References

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